SQUARE PULSE LTD

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Abstract

The usual LTD architecture [1, 2] provides sine shaped output pulses that may not be suitable in flash radiography, high power microwave production, z-pinch drivers, and certain other applications. A more suitable driver output pulse would have a flat or inclined top (slightly rising or falling). In this paper, we present the design and first test results of an LTD cavity that generates this type of output pulse by including within its circular array some number of third harmonic bricks in addition to the main bricks.

I. INTRODUCTION

The idea of the Square Pulse LTD is based on the Fourier theorem, which states that any waveform can be duplicated by the superposition of a series of sine and cosine waves. In particular, the constant function *f(x)* defined as

$$f(x)=\frac{\pi}{4} \qquad (1)$$

at $0 \le x \le \pi$, can be duplicated by

$$f(x)=\sum_{p=1}^{\infty}\frac{\sin(2p-1)x}{2p-1}. \qquad (2)$$

Figure 1 shows how the equation (2) transforms into (1) depending on *p*. For the case $p = 2$ the equation (2) gets the form

$$f_2(x)=\sin x+\frac{\sin 3x}{a}, \qquad (3)$$

where $a = 3$. If a increases from 3 to ~9, the top of the pulse flattens, as this is shown in Fig. 2.

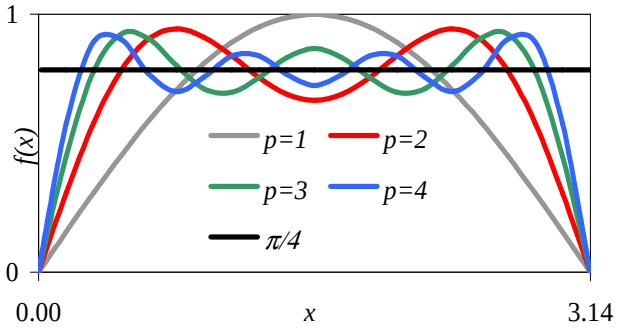

Figure 1. The function *f(x)* given by Eq. (2) at $p = 1 \div 4$ compared to $f(x) = \pi/4$.

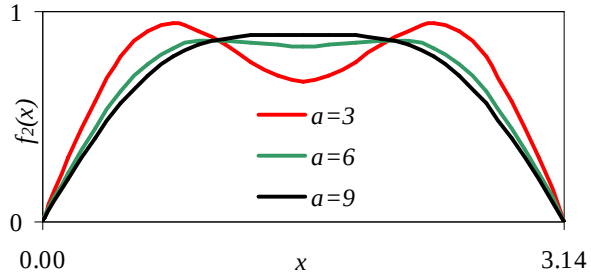

Figure 2. The function $f_2(x)$ depending on *a*.

If the function $f_2(x)$ is the current in the load, then to square the pulse at p=2, the driving circuit has to deliver to the load two sine pulses with different frequencies, ω_1 and $\omega_2 \sim 3\omega_1$, and the amplitude of the current pulse with the frequency ω_2 has to be ~9 times less than that the one with the frequency ω_1, depending on the requirements to the shape of the pulse. The LTD architecture is

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convenient for such kind of pulse shaping because its discharge circuit is composed of multiple separate bricks connected in parallel. The output LTD pulse can be squared as in Fig. 2 if the bricks in the cavity are of two different kinds: part of them are standard "1ω" bricks that deliver the main energy into the load, and the other part are modified "3ω" bricks that flatten the top of the output pulse.

II. ESTIMATION OF THE SQUARE PULSE LTD PARAMETERS

The simplified scheme of the square pulse LTD is shown in Fig. 3. Here C_1, L_1 and R_1 are total capacitance, inductance and resistance of the standard brick, the number of these bricks in the cavity is s. Similarly C_2, L_2 and R_2 denote the parameters of the modified brick, the number of the modified bricks is m. All bricks are connected in parallel and triggered simultaneously at t = 0. The resistance R_C simulates the energy loss in the core, L_L and R_L are the inductance and the resistance of the cavity load. We assume also that both standard and modified bricks are charged to same charge voltage U_0, as this is preferable in the real cavity.

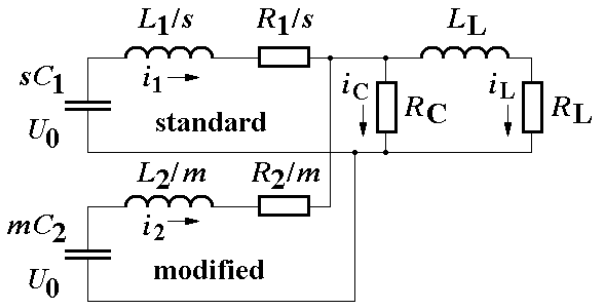

Figure 3. Simplified electrical scheme of the Square Pulse LTD.

The circuit equations describing the scheme in Fig. 3 at $t \geq 0$ are the following:

$$\begin{cases} U_0 = \dfrac{1}{sC_1}\displaystyle\int_0^t i_1 dt + \dfrac{L_1}{s}\dfrac{di_1}{dt} + \dfrac{R_1}{s} i_1 + R_C i_C , \\ U_0 = \dfrac{1}{mC_2}\displaystyle\int_0^t i_2 dt + \dfrac{L_2}{m}\dfrac{di_2}{dt} + \dfrac{R_2}{m} i_2 + R_C i_C , \\ R_C i_C = L_L \dfrac{di_L}{dt} + R_L i_L , \\ i_1 + i_2 = i_C + i_L , \end{cases} \qquad (4)$$

where $i_1(t)$ is the current flowing in the standard bricks, $i_2(t)$ the current in the modified bricks, $i_C(t)$ the current in the resistance R_C, and $i_L(t)$ the current in the load R_L. All these currents are zero at t = 0. At arbitrary set of the parameters, the system (4) does not have analytical solution. Fortunately, for our current purposes the approximate solution of this system in quite certain conditions is enough. These conditions are:

i) since the standard bricks store the main energy, they have to be matched with the cavity load, i.e. the following condition has to be satisfied:

$$\sqrt{\frac{L_1 / s}{sC_1}} = \frac{1}{s}\sqrt{\frac{L_1}{C_1}} = \frac{1}{s}\rho_1 \sim R_L . \qquad (5)$$

ii) to square the output pulse, the circuit frequency of the modified bricks has to be ~3 times higher than that of the standard bricks, i.e.

$$\sqrt{L_1 C_1} \sim 3\sqrt{L_2 C_2} . \qquad (6)$$

iii) in standard fast LTDs, the bricks are designed in such a way that for the given capacitors and switches, the inductance L_1 is already reduced to its minimal possible value. This means that the inductance L_2 is limited, at least from the bottom, by the value

$$L_2 \sim L_1 . \qquad (7)$$

When Eq. (7) is satisfied, Eq. (6) results in

$$C_1 \sim 9C_2 , \text{ and } \rho_2 = \sqrt{\frac{L_2}{C_2}} \sim 3\rho_1 . \qquad (8)$$

Simulations of the circuit presented in Fig. 3 indicate that, if the Eqs. (5)-(7) are satisfied, the standard and modified bricks discharge into the load R_L as if they werealmost independent on each other. This provides simple understanding of how to design the square pulse LTD depending on the desired shape of the output pulse. In particular, the shape of the top part of the pulse should depend on relative number of the standard bricks in the cavity, s/m, because (see Eq. (3) and Fig. 2)

$$a = \frac{I_1}{I_2} \sim \frac{s}{m}\frac{\rho_2}{\rho_1} \propto \frac{s}{m} , \qquad (9)$$

where I_1 and I_2 are the amplitudes of the currents delivered by the standard (I_1) and the modified bricks (I_2) into the load R_L.

III. DESIGN AND DIAGNOSTICS OF THE SQUARE PULSE LTD

The Square Pulse LTD was designed consisting of s = 6 standard bricks each of two series GA 35460 (100 kV, 8 nF) capacitors, and m = 2 modified bricks each of four

series TDK ceramic capacitors type UHV-12A (50 kV, 1.7 nF). Since the capacitance of the GA capacitors is ~8.4 nF = $2C_1$, at L_1 ~ 300 nH and s = 6, the cavity matched load was expected to be R_L ~ 1.4 Ohm. Such cavity load means that each of the two modified bricks is loaded into the resistance R_m ~ $2R_L$ ~ 2.14 Ohms. If the Eq. (7) is satisfied, then R_m ~ 2.14 Ohm is well below the matched load for the modified bricks:

$$\rho_m \sim \sqrt{\frac{L_2}{C_2}} \sim \sqrt{\frac{300\text{nH}}{1.7\text{nF}/4}} \sim 27 \text{ Ohms} >> R_m, \quad (10)$$

and the current in these bricks would oscillate, as required.

The layout of the Square Pulse LTD with 6 standard and 2 modified bricks is presented in Fig. 4, showing the bottom raw of the capacitors in the bricks. In tests described below the number of the standard bricks was varied in order to compare test results with simulations.

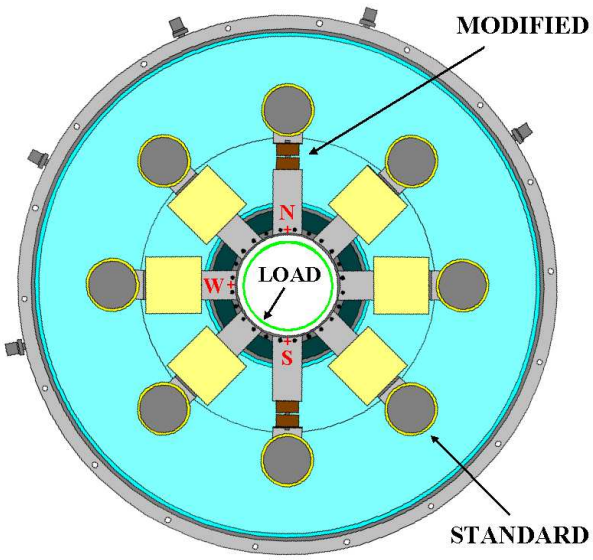

Figure 4. Square Pulse LTD with 6 standard and 2 modified bricks.

Figure 5 shows the design of the modified and standard bricks in this cavity. In both bricks same multigap switches with corona discharge [3-4] are used allowing firing these bricks simultaneously when their capacitors are charged to the same total voltage.

The cavity core is made of ET3425 iron tape with the thickness δ = 80 μm, the length of its center line is ℓ ~1.2 m. It consists of 6 rings; total cross section of iron in these rings is S ~53 cm^2. At passive premagnetization, which was used in the tests described below, the voltsecond integral of this core is VS_{CORE} ~17 mVs.

The cavity load is made as a 10-mm-wide, 124-mm-long circular cavity filled with KBr water solution of proper concentration. The position of this cavity is shown in Fig. 4 in green. The current flowing in the load was measured by using 3 differential-output B-dot monitors similar to those described in [7]. Red crosses marked as N, W, and S indicate the location of these monitors relative to the position of the standard and modified bricks in the cavity.

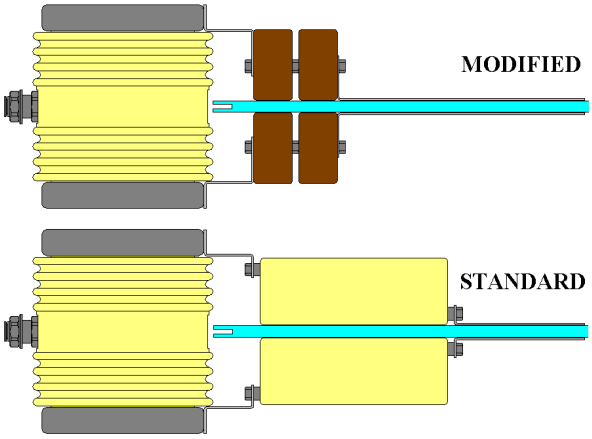

Figure 5. Modified brick with TDK ceramic capacitors and standard brick with GA 35460 oil-filled capacitors.

The load voltage was measured by using the external oil-filled resistive voltage divider. The input of this divider locates in the center of the cavity load, thus it was measuring the load voltage which is averaged along the load circumference.

IV. PSPICE SIMULATION

The Pspice schematics used to simulate the Square Pulse LTD is presented in Fig. 6. It consists of s=6 standard and m=2 modified bricks. In each standard brick the capacitance of two series GA capacitors is 4.13 nF, their resistance is 1.2 Ohms. The capacitance of four series TDK capacitors in the modified brick is 0.425 nF, their resistance is also 1.2 Ohms.

The switches in the bricks are simulated by using the blocks swxBR_1-8, whoseschematics is shown in Fig. 7. It simulates the current-dependent resistance of the switches [5] to take into account the influence of the rather different currents flowing in the standard and modified bricks.

The inductance of the standard brick is ($L1$+$L12$)=193 nH. It is divided in 2 parts, $L1$=180 nH is the inductance of two GA capacitors and the switch loop, $L12$=13 nH the inductance of the strip line connecting the capacitors with the AK gap of the cavity. The inductance of the modified brick is ($L2$+$L22$)=207 nH, $L2$=190 nH is the inductance of four series TDK capacitors and the switch loop, $L22$ =17 nH the inductance of the strip line connecting the TDK capacitors with the AK gap of the cavity.

The inductance of the load cavity is *LL* = 2.6 nH, and *RL* is the load resistance.

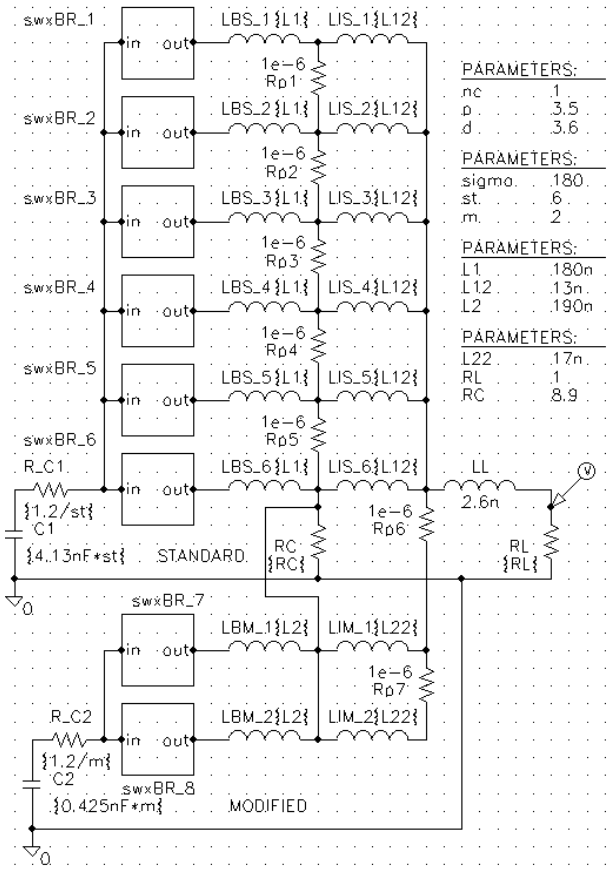

Figure 6. Pspice schematics of the Square Pulse LTD.

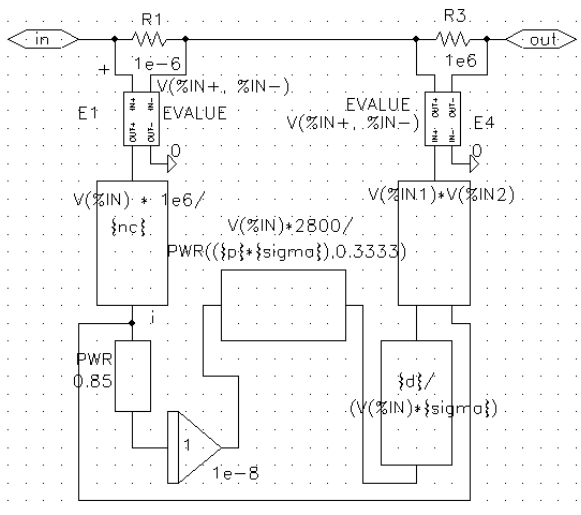

Figure 7. Schematics of the blocks swxBR_1-8 in Fig. 6.

The core is simulated as a resistance *RC* connected in parallel to the output strip lines. According to [6], the energy loss in this resistance is given by

$$RC \sim 8\frac{\rho S}{\ell\delta^2}\frac{\Delta B}{\Delta B(\tau)}, \qquad (11)$$

where ρ = 5×10^{-7} Ohm.m is the specific resistivity of ET3425 iron, ΔB = 3.2 T is the induction swing of ET3425 iron at passive premagnetization, and

$$\Delta B(\tau) = \frac{1}{S}\int_0^{\tau} U(t)dt \qquad (12)$$

is the induction swing produced in the core by the τ- long voltage pulse *U(t)*. It is the same as the energy loss due to generation of the Eddy current in the actual core. In terms of the voltsecond integrals, Eq. (11) gets the form

$$RC \sim 8\frac{\rho S}{\ell\delta^2}\frac{VS_{CORE}}{VS_{PULSE}} \sim \frac{46.75}{VS_{PULSE}\ [\text{mVs}]}\ \text{Ohms}, \qquad (13)$$

where VS_{PULSE} is the voltsecond integral applied to the core. This integral depends on the number of the standard bricks *s* in the cavity and the load resistance *RL*, for each given *s* and *RL*. The value of VS_{PULSE} and the resistance *RC* were defined in simulations by using the iteration process.

The resistors Rp1-7=10^{-6} Ohms are introduced into the schematics in Fig. 6 instead of the wires, they are needed to break the inductor loops, as this is required in Pspice.

Simulated load voltage at *RL*=1 Ohm (which is the peak power load for the schematics in Fig. 6) at 200 kV total charge voltage on the capacitors is shown in Fig. 8. The self-consistent values of the voltsecond integral VS_{PULSE} and the resistance *RC* for this load are 5.25 mV s and 8.9 Ohm, respectively. The peak load voltage is ~73 kV, its width at 90% of maximum is ~42 ns compared to ~99 ns at 10% of maximum.

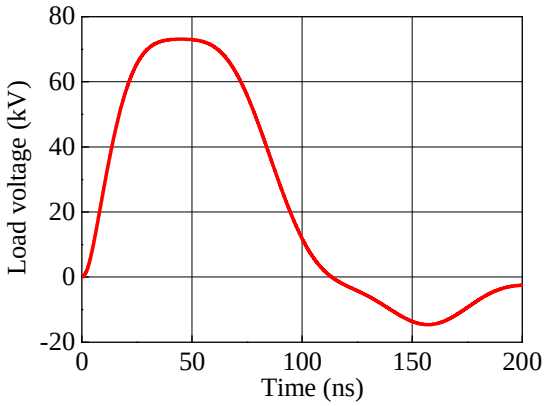

Figure 8. Simulated load voltage at *RL* =1 Ohm at 200 kV charge voltage on the capacitors.

The energy delivered to *RL* =1 Ohm during the main pulse (in ~110 ns) is 317 J or ~62% of 512 J stored in the capacitors. The energy loss in the switches of the standard bricks is ~12%, in the resistance of the GA capacitors ~15%, and in the core ~7%. The energy loss in the switches of the modified bricks is 6.55 J or ~1.3% of the total stored energy but ~39% of the energy stored in the TDK capacitors of the modified bricks.

V. TEST RESULTS

To the moment the Square Pulse LTD was tested with m=2 modified and s=2 or 4 standard bricks. In these tests, the modified bricks were located opposite to each other, on the diameter going through the positions of the B-dot probes marked by "N" and "S" in Fig. 4. In tests with 2 standard bricks, these bricks were located symmetrically between the modified bricks on the diameter going through the position of the B-dot probe marked by "W". In tests with 4 standard bricks, these bricks were located in pairs on opposite sides on the cavity evenly between the modified bricks. Thus in tests with 4 standard bricks, the B-dot probe marked by "W" in Fig. 4 was located between the two left standard bricks.

The resistance of the load was defined as $R_L=U_L/I_L$, where U_L is the load voltage recorded by the external voltage divider, and I_L is the load current calculated as

$$I_L = 0.5I_{\mathrm{W}} + 0.25I_{\mathrm{N}} + 0.25I_{\mathrm{S}}, \qquad (14)$$

where I_{W}, I_{N}, and I_{S} are integrated signals from the B-dot probes marked by "W", "N" and "S", respectively.

Figure 9 shows the recorded and simulated (VS_{PULSE} =3.34 mVs, RC=14 Ohms) load voltage at s=m=2, R_L=1.65 Ohms, at a charge voltage U_{CH} = ±96 kV. It indicates that the presence of the modified bricks alters the shape of the LTD pulse in proper direction, and the simulation is correct within few percents.

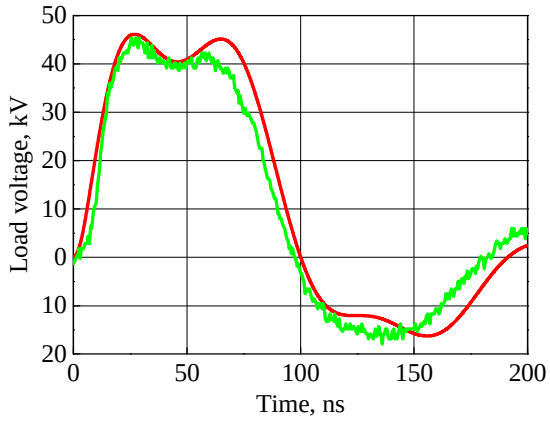

Figure 9. Recorded (in green) and simulated (in red) load voltage at s=m=2, R_L=1.65 Ohms, at U_{CH} =±96 kV.

Fig. 10 presents the load current I_L compared with the currents measured by separate B-dot probes in same shot as the one presented in Fig. 9. The shape of the I_N and I_S currents in front of the modified bricks is similar, both with two peaks, whereas the current I_W measured in front of the standard brick peaks only once. This indicates that the currents from the standard and modified bricks in the given design of the stage do not distribute evenly around the whole circumference of the load cavity.

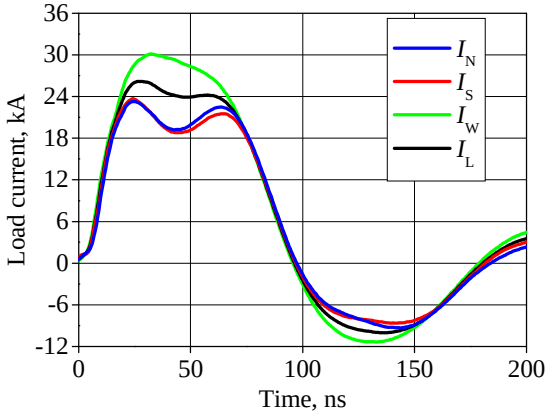

Figure 10. Load current measured by separate B-dot probes, and the total load current I_L calculated by using Eq. 14. Same shot as that in Fig. 9.

Figure 11 shows the recorded and simulated (VS_{PULSE} =5.2 mV s, RC=8.99 Ohms) load voltage at s=4, m=2, R_L=1.55 Ohms, and U_{CH} =±100 kV. In this case, the two peaks merge into quasi flat top of the pulse. The load current measured by separate B-dot probes and the total load current I_L are shown in Fig. 12. Again, the currents I_N and I_S are close to each other, and less than the current I_W.

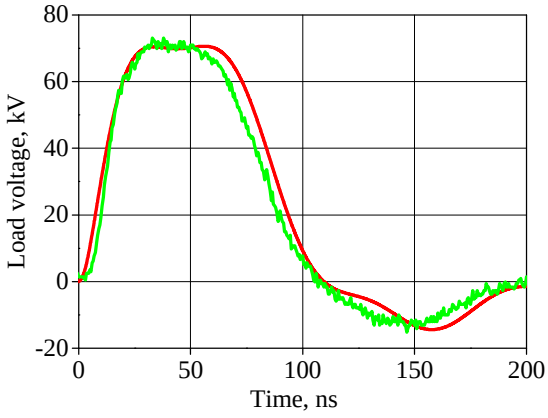

Figure 11. Recorded (in green) and simulated (in red) load voltage at s=4, m=2, R_L=1.55 Ohm, at U_{CH} =±100 kV.

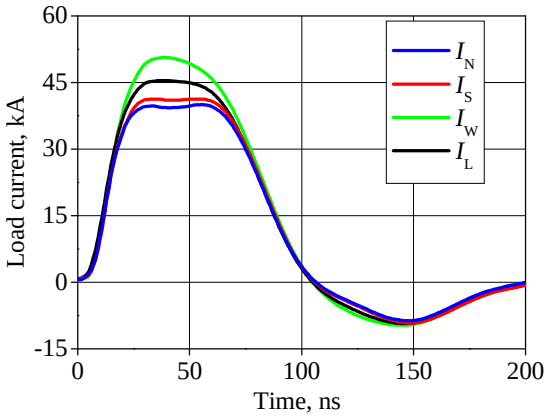

Figure 12. Load current measured by separate B-dot probes, and the total load current I_L calculated by using Eq. 14. Same shot as that in Fig. 11.

In order to verify the validity of the Eq. 13 for simulation of the energy loss in LTD cores, the top metal flange of the stage was replaced with a plastic one thus breaking the current loop around the core. For the schematics in Fig. 6 this means that the resistance of the core, *RC*, becomes infinitely large and no energy can be lost in the core. Fig. 13 demonstrates the recorded load voltage trace in this test at s=4, m=2, RL=1.65 Ohm, U_{CH} =±100 kV in comparison with the simulated one at RC = 10^6 Ohm. Both curves are very close thus confirming the validity of the Eq. 13 for estimation of the energy loss in LTD cores.

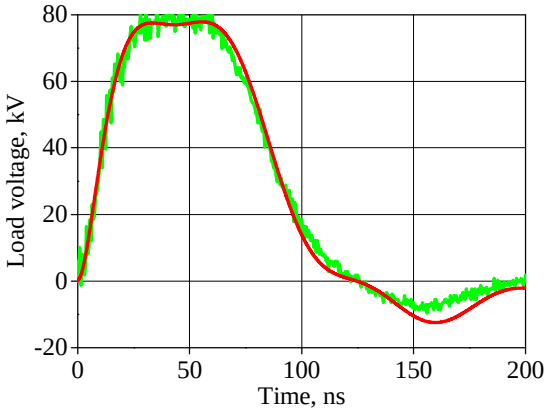

Figure 13. Recorded (in green) and simulated (in red) load voltage at s=4, m=2, R_L=1.65 Ohm, at U_{CH} =±100 kV. The current loop around the core is broken, the resistance of the core is set to RC =10^6 Ohm.

VI. CONCLUSION

The results presented in this report definitely indicate that the shape of the output LTD pulse can be squared if the cavity is assembled with some number of modified bricks with ~10 times less capacitive storage capacitors than in the standard bricks. Relative number of the modified bricks determines the shape of the output pulse.

The top of the output pulse can be made flat, but also it can be made rising or falling down depending on the parameters of the discharge circuit, in particular, on the ratio between the total inductance of the standard and modified bricks. This opens the way to generate the output pulses that are most preferable for different applications.

VII. ACKNOWLEDGEMENTS

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VIII. REFERENCES

[1] A. A. Kim, M. G. Mazarakis, V. A. Sinebryukhov, et.al., “Development and tests of the 1-MA linear transformer driver stages”, Phys. Rew. ST Accel. Beams **12**, 050402 (2009).

[2] M. G. Mazarakis, W. E. Fowler, A. A. Kim, et.al., “High-current, 0.5-MA, fast, 100-ns, linear transformer driver experiments”, Phys. Rew. ST Accel. Beams **12**, 050401 (2009).

[3] A.A. Kim, B.M. Kovalchuk, A.N. Bastrikov, et.al., “100 ns current rise time LTD stage”, in Proc. 13th IEEE Inter. Pulsed Power Conf., 2001, p. 1491.

[4] J.R. Woodworth, J.A. Alexander, F.R. Gruner, et.al., “Low-inductance gas switches for linear transformer drivers”, Phys. Rew. ST Accel. Beams **12**, 060401 (2009).

[5] A.A. Kim, V.G. Durakov, S.N. Volkov, et. al., “Gas switch performance depending on current in the circuit”, in Proc. 14th Symp. High Current Electronics, Tomsk 2006, p.297.

[6] A.A. Kim, M.G. Mazarakis, V.I. Manylov, et.al., “Energy loss due to eddy current in linear transformer driver cores”, Phys.Rev. ST Accel. Beams, **13**, 070401(2010).

[7] T.C. Wagoner, W.A. Stygar, H.C. Ives, et.al., “Differential-output B-dot and D-dot monitors for current and voltage measurements on a 20-MA, 3-MV pulsed power accelerator”, Phys. Rew. ST Accel. Beams **11**, 100401 (2008).